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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448	
75	90 08/16/2006		EXAM	INER	
ON Semiconductor			NADAV, ORI		
Patent Adminis	tration Dept - MD A700		·		
P.O. Box 62890 ART UNIT PAPE				PAPER NUMBER	
Phoenix, AZ	35082-2890		2811		
			DATE MAILED: 08/16/2006		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	——————————————————————————————————————		
	10/072,145	AVERETT ET AL.			
Office Action Summary	Examiner	Art Unit			
	Ori Nadav	2811			
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	correspondence addre	SS		
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory period v  - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be tire will apply and will expire SIX (6) MONTHS from the cause the application to become ABANDONE	N. nely filed the mailing date of this comm D (35 U.S.C. § 133).	·		
Status					
<ol> <li>Responsive to communication(s) filed on 13 Ju</li> <li>This action is FINAL.</li> <li>Since this application is in condition for allower closed in accordance with the practice under E</li> </ol>	action is non-final.  nce except for formal matters, pro		erits is		
Disposition of Claims					
4) ☐ Claim(s) 1,5-10,26,27,29,32 and 33 is/are pend 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) 1,5-10,26,27,29,32 and 33 is/are rejection is/are objected to. 8) ☐ Claim(s) is/are object to restriction and/or	vn from consideration.				
Application Papers					
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acce Applicant may not request that any objection to the of Replacement drawing sheet(s) including the correction 11) The oath or declaration is objected to by the Ex	epted or b) objected to by the liderating or b) objected to by the liderating of the drawing of	e 37 CFR 1.85(a). jected to. See 37 CFR 1	` '		
Priority under 35 U.S.C. § 119					
<ul> <li>12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</li> <li>a) All b) Some * c) None of:</li> <li>1. Certified copies of the priority documents have been received.</li> <li>2. Certified copies of the priority documents have been received in Application No</li> <li>3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</li> <li>* See the attached detailed Office action for a list of the certified copies not received.</li> </ul>					
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	ite	2)		

Art Unit: 2811

## **DETAILED ACTION**

# Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-10 and 26-33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitations of at least a portion of the semiconductor (cap) layer is configured to convert to a semiconductor oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is exposed to an oxidizing environment, as recited in claims 1 and 26, respectively, are unclear as to whether the intermediate structure has a portion of the semiconductor (cap) layer being a semiconductor oxide, and if so, the location of this new layer with respect to the intermediate structure. It is further unclear whether the semiconductor substrate is exposed to an oxidizing environment, and the resulting structure of such exposure.

#### Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

semiconductor substrate:

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6-8, 26, 29 and 32, as best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Mandelman (6,518,641).

Regarding claims 1 and 26, Mandelman teaches in figure 1G and related text an intermediate semiconductor device, comprising:

a semiconductor substrate 10 having a surface formed with a first recessed region S1;

a first dielectric material 22 formed in the first recessed region;

a second recessed region S2 formed within the first dielectric material, wherein the second recessed region has walls, a lower surface and a first opening in proximity to the surface; and

a semiconductor layer 35 formed overlying the first dielectric material 22 having a second opening at least partially over the first opening, wherein at least a portion of the semiconductor layer is configured to convert to a semiconductor oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is exposed to an oxidizing environment.

Regarding claims 6-8, 29 and 32, Mandelman teaches in figure 1G and related text, wherein the first dielectric material includes deposited silicon dioxide, and a layer of material 40 formed overlying the walls of the second recessed region, wherein the first dielectric material is recessed below a major surface of the

# Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 9-10, 27 and 33, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Mandelman (6,518,641).

Regarding claims 5, 10, 27 and 33, Mandelman teaches in figure 1G and related text substantially the entire claimed structure, as applied to claims 1 and 26 above, except stating that the semiconductor (cap) layer is configured to convert to a semiconductor oxide comprises polysilicon. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a polysilicon semiconductor (cap) layer to convert to a semiconductor oxide in order to simplify the processing steps of making the device by using a conventional method of forming a semiconductor oxide.

Regarding claim 9, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recess the first dielectric material below the major surface a distance of about 0.5 microns in prior art's device in order to adjust the characteristics of the device according to the requirements of the application in hand.

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Regarding claim 28, the process limitations of "thermally grown silicon dioxide" would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

### Response to Arguments

Applicant's arguments with respect to claims 1, 5-10, 26-27, 29 and 32-33 have been considered but are most in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660.

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The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N. 8/7/06 ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800

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